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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,641	12/16/2003	Shorin Kyo	Q78967	3524

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EXAMINER	
SHIKHMAN, MAX	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,641	KYO, SHORIN	
	Examiner	Art Unit	
	Max Shikhman	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/19/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/19/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicants' response to the last Office Action, filed 07/19/2007 has been entered and made of record.

Claim Objections

2. Claim 13 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 1 already ignores the center column.

In Claims 4,8,12, remove the brackets around P and Q, please.

Appropriate correction required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

() Regarding Claims 1,5,9:

Claim 1 almost last line, "...*calculates pixel values of said image*".

Pixel values of the original image data are already known.

"...*calculates pixel values of said image data by cumulatively adding said intermediate data.*"

"*cumulatively adding*" results in one value. How does this one value calculate many *pixel values*? Which pixel values are being calculated? For example, a filter can replace a center pixel with an average of its 3x3 neighborhood. Claim 1 does not replace anything.

Claim 1 recites (on last line), "*cumulatively adding said intermediate data*", which would be understood to add at least two of the intermediate data. But operating means already "*cumulatively adds the multiplied results*" which should generate only a single value.

Claim 1 recites the limitation "*operation results*". There is insufficient antecedent basis for this limitation in the claim. "*operation results*" could mean "*multiplied results*" or after cumulative addition of the multiplied results or something else.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-16 rejected under 35 U.S.C. 103(a) as being unpatentable over

Gonzalez, "Digital Image Processing, 2/E" (ISBN-10: 0201180758. Published: 11/09/2001) in view of

Morris Mano, "Computer System Architecture" (Prentice Hall; 3 edition. ISBN-10: 0131755633.)

() **Regarding Claims 1,5,9 and 3/1,7/5,11/9**:

For Claim 5, *A computer-readable storage medium storing a program for making a computer work* (P117 Formula (3.5-1) is in digital form. P29 Fig1.24 shows a computer and software.)

A symmetric type image filter (Fig 3.34) *processing apparatus, which processes image data by a symmetric type image filter composed of* $N \times M$ *kernel coefficients* (Fig 3.34 [w(s,t)]) *N and M are odd numbers being 3 or more integers, comprising:*

(Gonzalez, Page 117, Figure 3.32 and formula (3.5-1) show a mask w operating on the image f(x,y). Figure 3.32 shows a 3x3 mask. The mask can be symmetric by equating the left column to the right column, w(-1,-1)=w(-1,1) etc; Fig 3.34 shows symmetry.)

an operating means that multiplies [w*f] *kernel coefficients* [w(s, t)] *of one or more columns on the left or on the right* [w(s, ± 1)] *of a center column* [w(s,0)]

(The case of t=0 can be excluded from multiplication by letting $t \neq 0$. (3.5-1) Summation is linear {p116}, some terms can be excluded, use $\sum_{t=-b, t\neq 0}^{t=b}$.

Alternatively, use $\sum_{t=-b, t\neq k}^{t=b}$ when w(s,k)=0, since these are zeros.)

by column elements of image data corresponding to said one or more columns

[f(x+s, y ± 1).]

and cumulatively adds the multiplied results;

(Formula (3.5-1), $\sum_{t=-b,t\neq 0}^{t=b}$)

a pixel value calculating means, that calculates pixel values of said image data [g(x,y)]

by cumulatively adding $\sum_{s=-a}^{s=a}$ *said intermediate data memorized in said memorizing means.*

Gonzalez discloses everything as described above except, *a memorizing means that memorizes operation results generated at said operating means as intermediate data;*

Mano, p327-328, Fig 9.15 shows "SIMD array processor organization". P327 shows "processing elements (PE), each having a local memory M...ALU and arithmetic unit." M1...Mn is memory. Each PE can multiply and add. As Mano says, P327 SIMD calculates in parallel for fast speed, with each processing unit PE working on one calculation. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Mano's SIMD processor for fast parallel computation. Each PE can calculate one multiplication or addition using Gonzalez' $\sum_{t=-b,t\neq 0}^{t=b}$. Mn can store the results. Fig 9.15 "Master control unit" or PE can then calculate Gonzalez' $\sum_{s=-a}^{s=a}$.

() **Regarding Claims 2,6,10**:

A symmetric type image filter processing apparatus in accordance with claim 1, wherein:

said operating means calculates intermediate data in one row (Gonzalez. $\sum_{s=-a}^{s=a}$. "s" controls rows) *of said image data,* [Gonzalez. g(x,y)]

and said pixel value calculating means reads out (Mano. Fig 9.15 "Master control unit") *said intermediate data* (Mano. Intermediate data is stored in Fig 9.15 M1...Mn) *corresponding to the position of each pixel of said image data,* [Gonzalez. g(x,y)]

and calculates said pixel value [Gonzalez. g(x,y)] *by cumulatively adding*

[Mano, p327-328, Fig 9.15 implementing Gonzalez' formula (3.5-1)]

said read out intermediate data.

(Mano. Fig 9.15 "Master control unit")

() **Regarding Claims 4,8,12**:

Limitations of claims 4,8,12 have been covered in claim 1 already. This is a review.

A symmetric type image filter processing apparatus in accordance with claim 1, wherein:

the number of pixels in one row of said image data is P (P is a positive integer), and

(Gonzalez. Fig 3.32 shows such an image.)

said operating means multiplies each kernel coefficient [P117. w(s, t)] of M (3) *pieces in each column of {(N + 1)/2}* (2) *columns at said right or left* [w(s, ± 1)] *of said center column* [w(s,0)]

(Gonzalez. The case of t=0 can be excluded from multiplication by letting $t \neq 0$. (3.5-1)

Summation is linear {p116}, some terms can be excluded, use $\sum_{l=-h, l\neq 0}^{l=h}$.

Alternatively, use $\sum_{l=-h, l\neq k}^{l=h}$ when w(s,k)=0, since these are zeros.)

by each pixel of M pieces in the column direction

[Gonzalez. f(x+s, y ± 1) are the two columns.]

of said image data and cumulatively adds the multiplied results,

(Gonzalez. Formula (3.5-1), $\sum_{l=-h, l\neq 0}^{l=h}$)

by using SIMD commands (Mano, p327-328, Fig 9.15 shows "SIMD array processor organization".) *that are capable of processing data of sequential Q* (Fig 9.15: n) *pieces simultaneously* (Mano, p327, "parallel") *(Q > 1 and Q is a positive integer satisfying the condition P > Q), and* (1<n<P)

executes this multiplying and cumulatively adding operation P / Q times,

(Mano p328. "Vectors of greater length than 64 must be divided into 64-word portions."

64 is an example value.)

and generates said intermediate data in one row of said image data.

(Gonzalez. $\sum_{s=-a}^{s=a}$. "s" controls rows.

Mano. Fig 9.15. PE1 to PEn generates in one row.)

() **Regarding Claim 13**:

The apparatus of claim 1, wherein said operating means utilizes less than all the N x M kernel coefficients during said multiplication.

(Gonzalez. P117 Fig3.32. N=M=3. Center column w(s,0) is ignored in claim 1 already.)

() **Regarding Claims 14,15,16**:

The apparatus of claim 1, wherein the pixel value calculating means stores the calculated pixel values of said image data in an operation result pixel storing region.

(Mano. P328 Fig 9.15. Mn.)

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7. **Claims 3/1, 7/5, 11/9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Mano as applied to Claims 1,5,9 above and further in view of Hsu, "Two-dimensional discrete cosine transform using SIMD instructions" (US-PAT-NO: 6973469).

() **Regarding Claim 3/1**:

Gonzalez discloses all of the subject matter as described above except, *operating means and said pixel value calculating means execute the operation of said multiplication and said cumulative addition by using SIMD commands.*

Hsu discloses as follows. (Column 2, lines 7-14), "For example, many processors now support single-instruction multiple-data (SIMD) commands ... Advanced Micro Devices, has proposed and implemented 3DNow!, a set of floating point SIMD instructions...".

(Column 2, lines 21-30) "SIMD commands are "vectored" instructions in which a single operation is performed on multiple data operands. Such instructions are very efficient for graphics and audio applications where simple operations are repeated..."

(Column 2, line 34) "Upon execution of a vectored multiply instruction..."

(Column 10, line 34-38) "Values from two columns are being processed in parallel by the multiplication, addition, and subtraction operations."

As Hsu discloses, it is efficient to implement repetitive instructions with SIMD commands; many processors support SIMD. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to add Hsu's method to Gonzalez's method, to use SIMD commands for multiplication and addition. This would allow the implementation of Gonzalez's method on an SIMD AMD processor, AMD-K6.RTM.-2, efficiently.

() **Regarding Claim 7/5**:

Gonzalez discloses all of the subject matter as described above except, *operating step and said pixel value calculating step execute the operation of said multiplication and said cumulative addition by using SIMD commands.*

Hsu discloses as follows. (Column 2, lines 7-14), "For example, many processors now support single-instruction multiple-data (SIMD) commands ... Advanced Micro Devices, has proposed and implemented 3DNow!, a set of floating point SIMD instructions...".

(Column 2, lines 21-30) "SIMD commands are "vectored" instructions in which a single operation is performed on multiple data operands. Such instructions are very efficient for graphics and audio applications where simple operations are repeated..."

(Column 2, line 34) "Upon execution of a vectored multiply instruction..."

(Column 10, line 34-38) "Values from two columns are being processed in parallel by the multiplication, addition, and subtraction operations."

As Hsu discloses, it is efficient to implement repetitive instructions with SIMD commands; many processors support SIMD. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to add Hsu's method to Gonzalez's method, to use SIMD commands for multiplication and addition. This would allow the implementation of Gonzalez's method on an SIMD AMD processor, AMD-K6.RTM.-2, efficiently.

() **Regarding Claim 11/9**:

Gonzalez discloses all of the subject matter as described above except, *multiplying operation and said cumulatively adding operation and said pixel value calculating operation are executed by using SIMD commands.*

Hsu discloses as follows. (Column 2, lines 7-14), "For example, many processors now support single-instruction multiple-data (SIMD) commands ... Advanced Micro Devices, has proposed and implemented 3DNow!, a set of floating point SIMD instructions...".

(Column 2, lines 21-30) "SIMD commands are "vectored" instructions in which a single operation is performed on multiple data operands. Such instructions are very efficient for graphics and audio applications where simple operations are repeated..."

(Column 2, line 34) "Upon execution of a vectored multiply instruction..."

(Column 10, line 34-38) "Values from two columns are being processed in parallel by the multiplication, addition, and subtraction operations."

As Hsu discloses, it is efficient to implement repetitive instructions with SIMD commands; many processors support SIMD. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to add Hsu's method to Gonzalez's method, to use SIMD commands for multiplication and addition. This would allow the implementation of Gonzalez's method on an SIMD AMD processor, AMD-K6.RTM.-2, efficiently.

Response to Arguments

8. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kyo (PGPUB-DOCUMENT-NUMBER: 20040098709) discloses, "Method, apparatus, and computer program for generating SIMD instruction sequence".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Max Shikhman whose telephone number is (571) 270-1669; FAX 571-270-2669. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Max Shikhman
9.24.2007

BRIAN WERNER
SUPERVISORY PATENT EXAMINER